

A Programmable MEMS-Based Clock Generator with Sub-ps Jitter Performance

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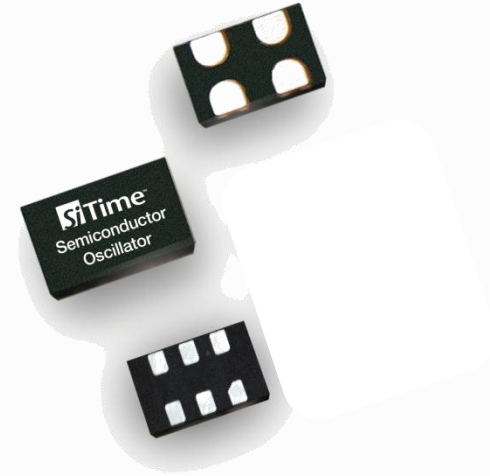
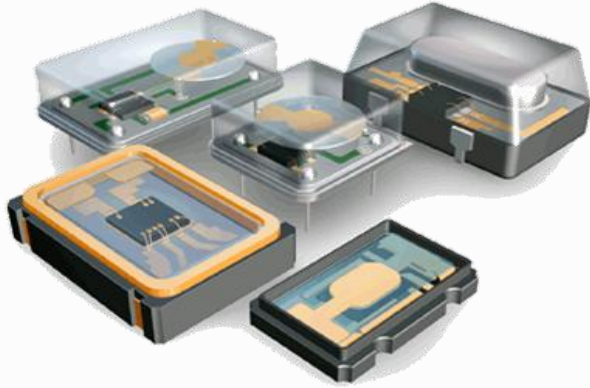
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Outline

- **Programmable MEMS-based Clock Generator**
- **Technical Challenges**
- **System Architecture**
- **Sub-ps Integrated Jitter PLL Development**
 - Architecture
 - Circuits
- **Measured Results**
- **Conclusion**

MEMS-based Clock Generators vs. Quartz Oscillators



Quartz Oscillators:

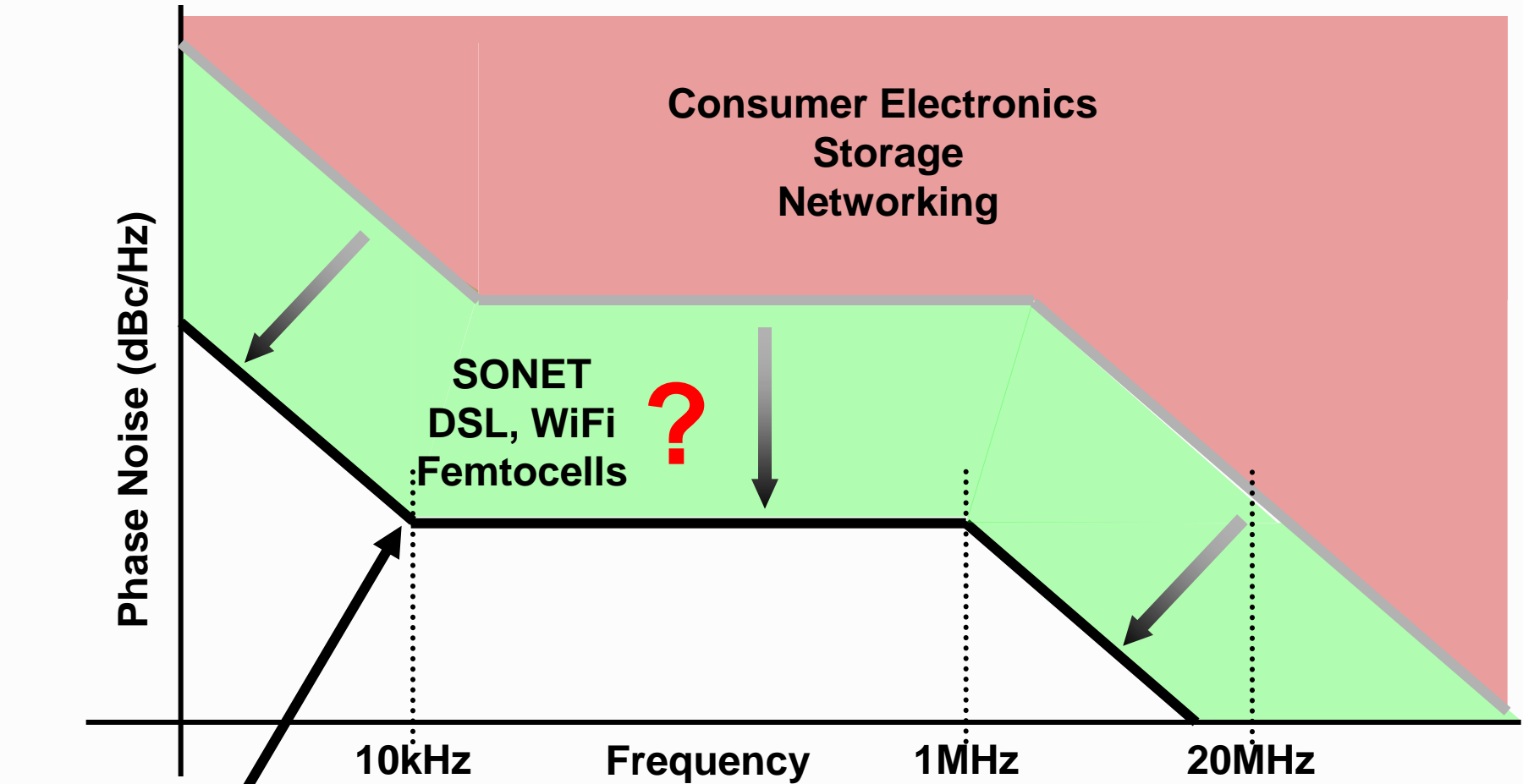
- **Ceramic or metal package**
- **Built in special processes**
- **Sensitive to shock & vibe**
- **Single frequency output**

MEMS-based Clock Generators:

- **Plastic QFN package**
- **Built in standard IC fabs**
- **Can withstand 50kg shock**
- **Multi-function/frequency out**

**MEMS has obvious advantages over Quartz.
What about performance?**

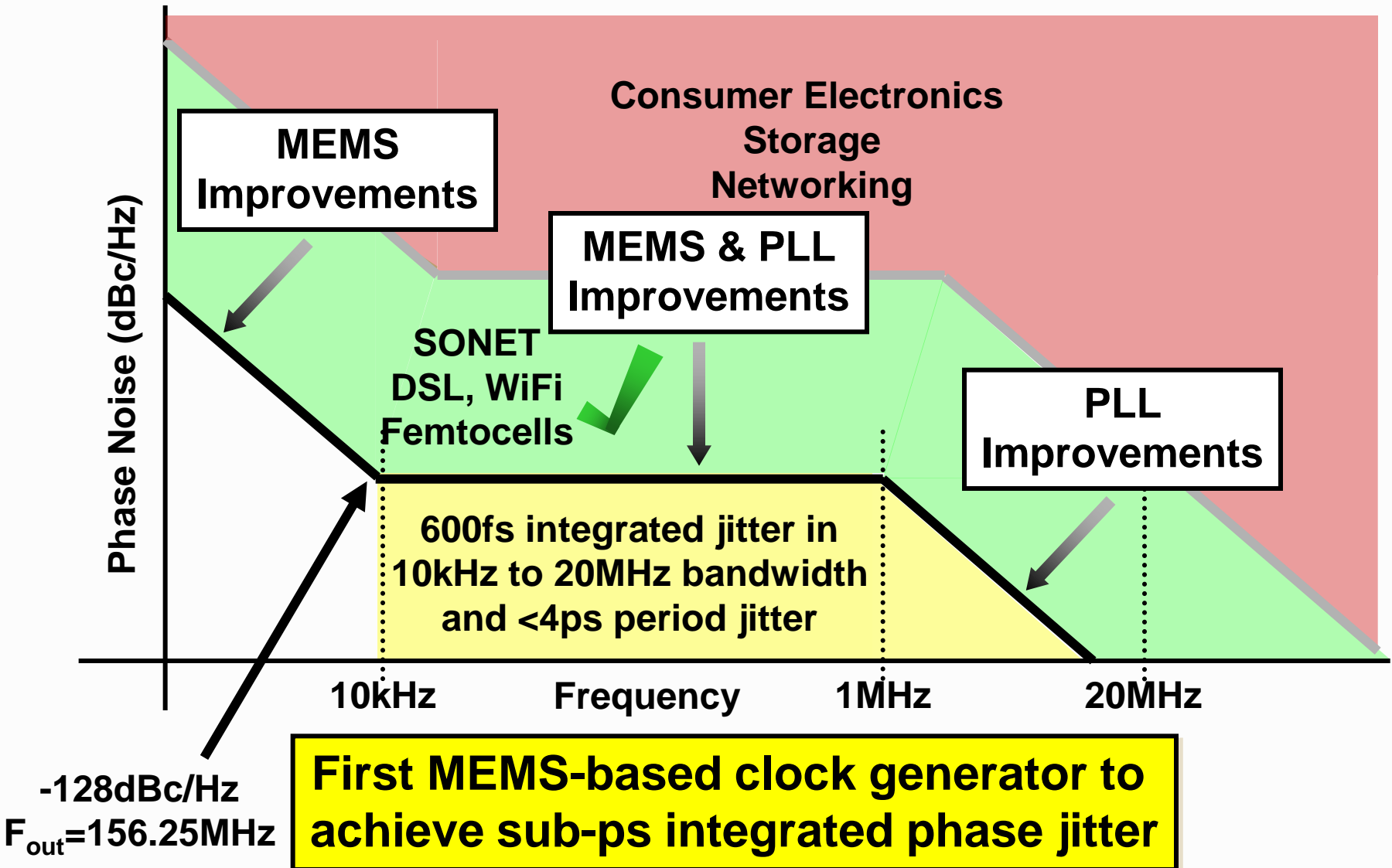
Technical Challenges



-128dBc/Hz
 $F_{out}=156.25\text{MHz}$

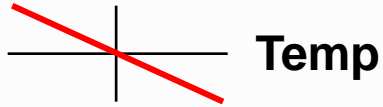
Can MEMS-based timing meet difficult timing requirements?

Technical Challenges

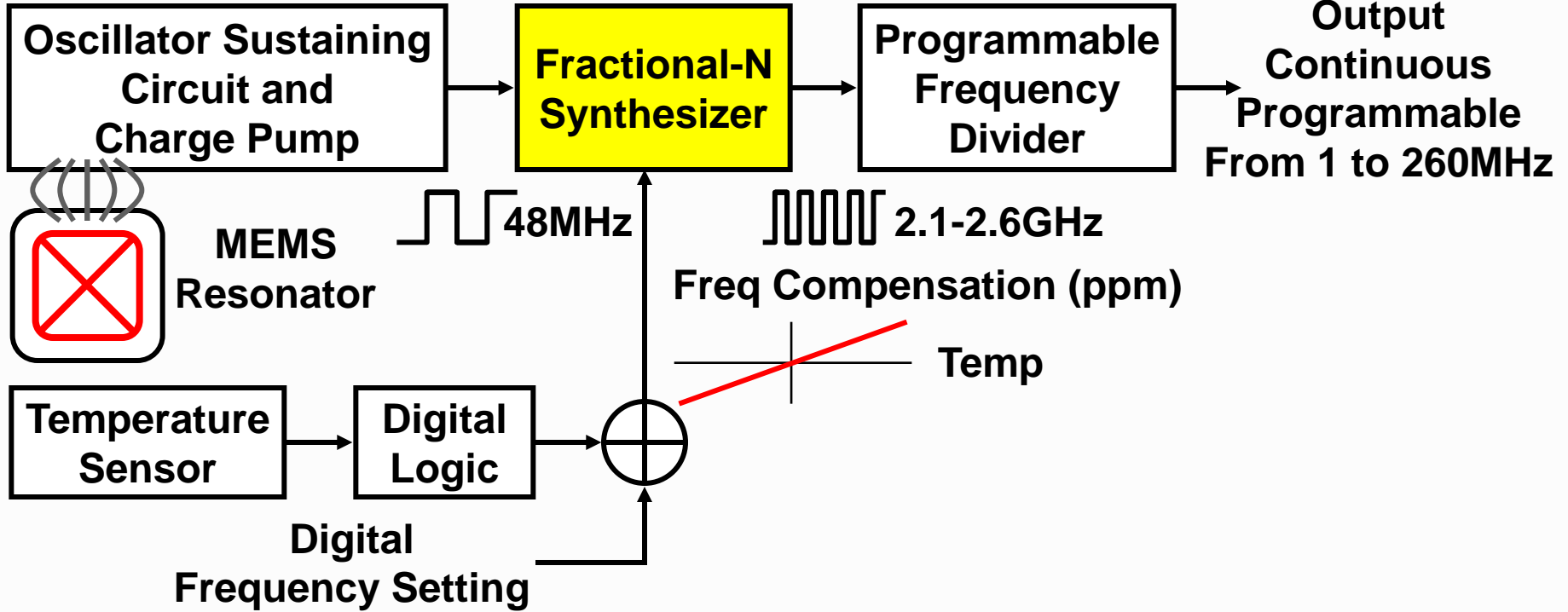


System Architecture

Freq Error (-30ppm/°C)

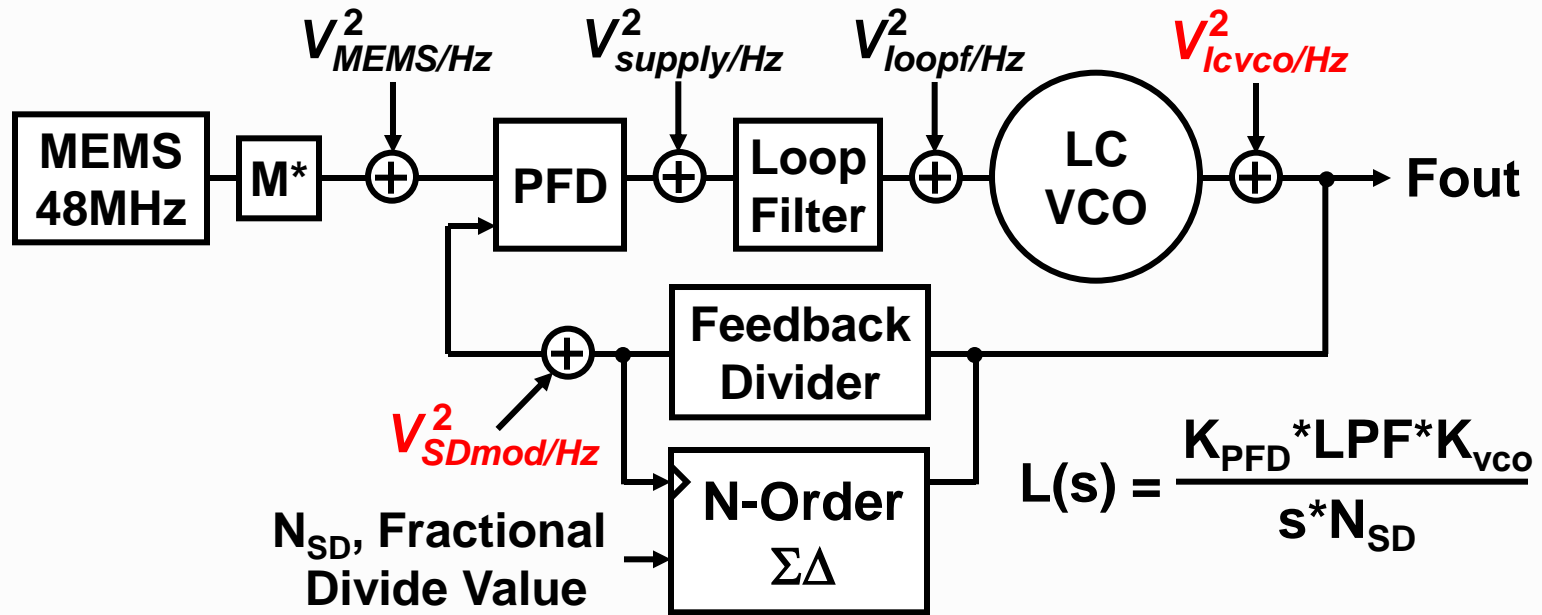


Freq Error (ppm)



MEMS -30ppm/°C frequency tempco easily compensated with temp sensor and frac-N synth

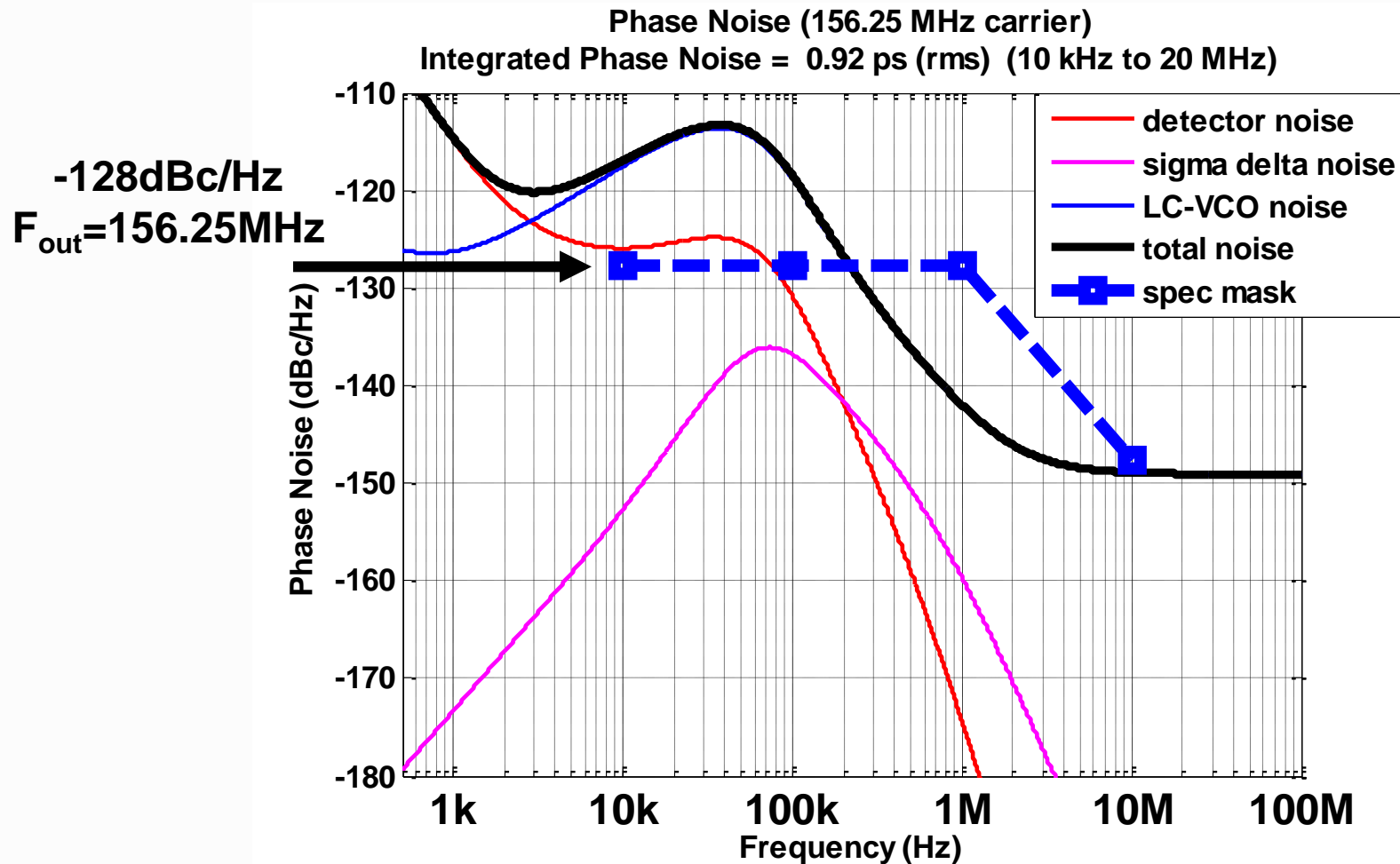
Sub-ps Integrated Jitter PLL Development



Assume:
 $M=1$
 $N\text{-order}=2$

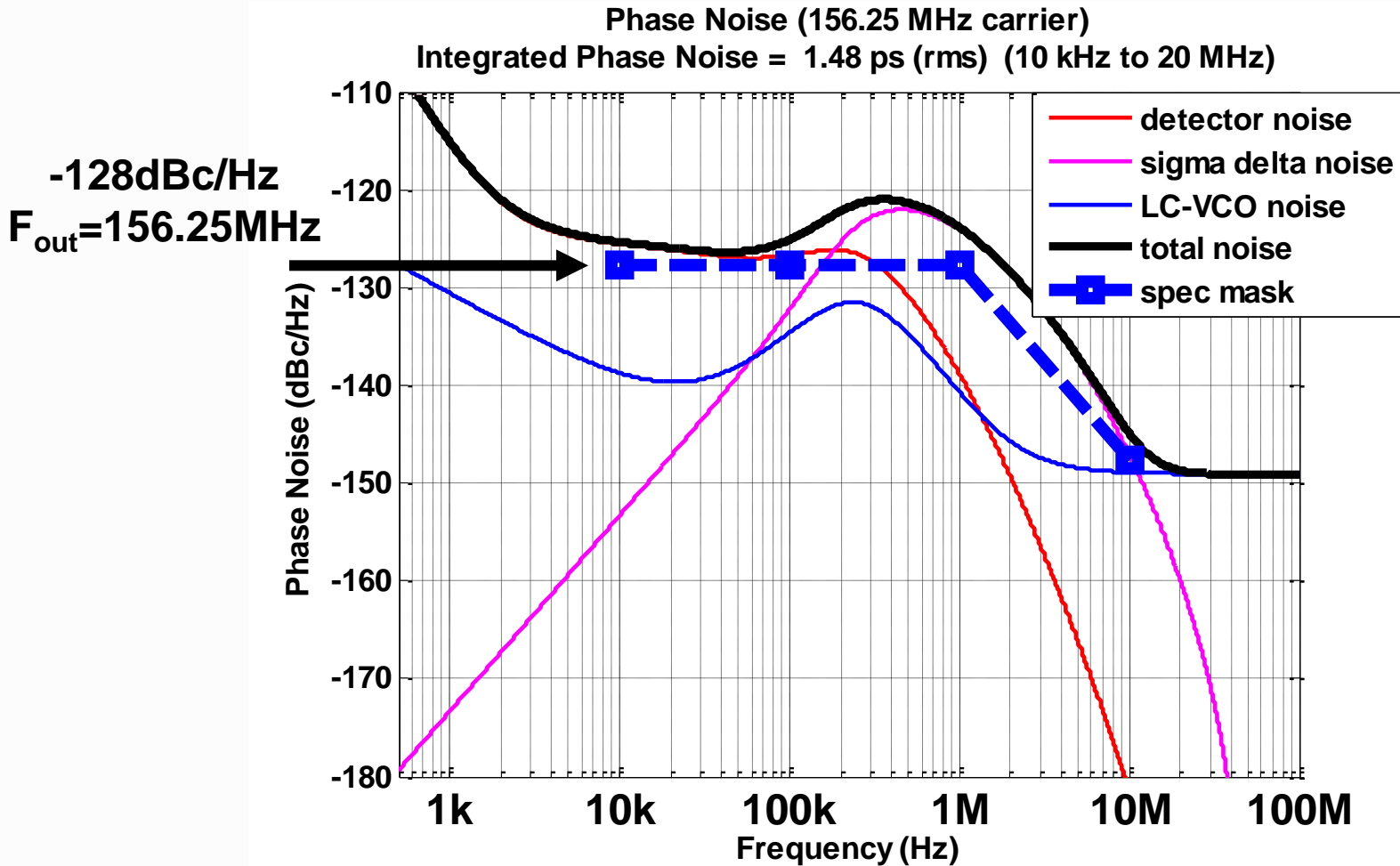
PLL bandwidth optimization critical for low integrated jitter and meeting mask requirement

Fractional-N PLL with low (80kHz) PLL BW



$\Sigma\Delta$ noise is suppressed
but phase noise dominated by VCO

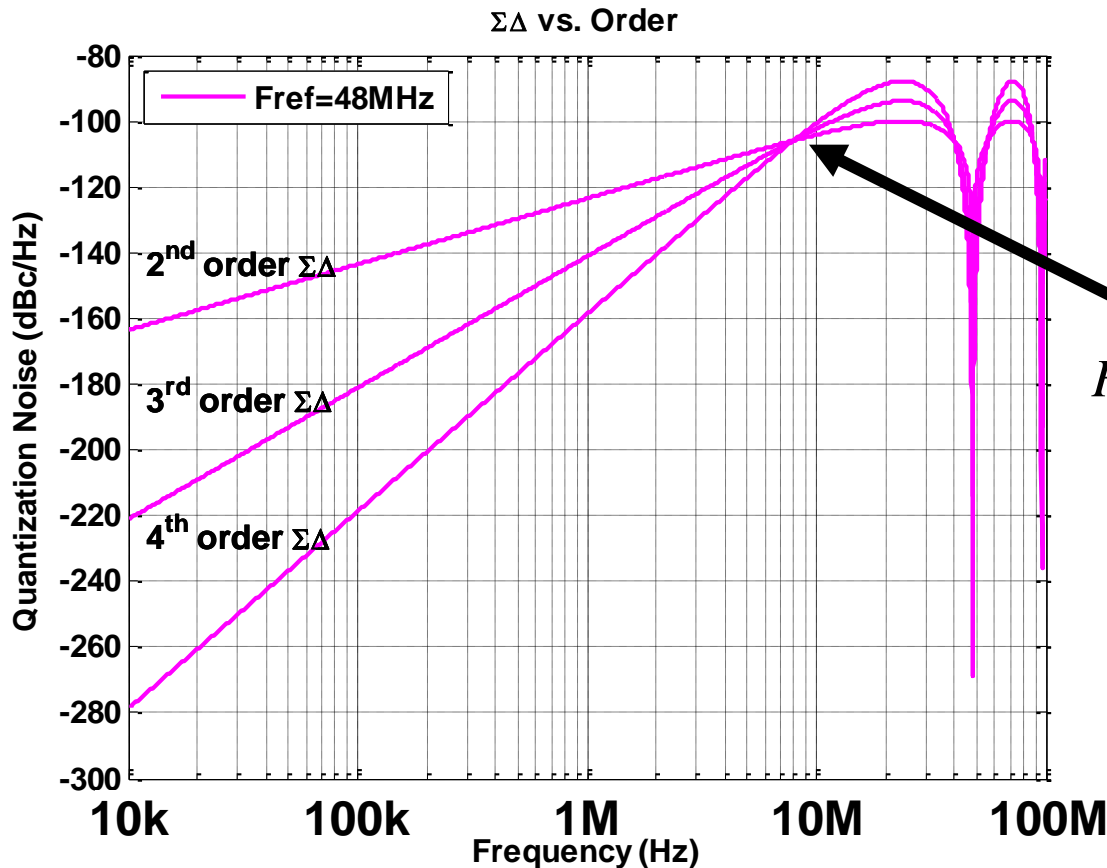
Fractional-N PLL with high (400kHz) PLL BW



**VCO noise is suppressed
but phase noise dominated by $\Sigma\Delta$**

What about $\Sigma\Delta$ Noise?

$$V_{SD\text{mod}/\text{Hz}}^2(s) = \frac{T_{REF}(2\pi)^2}{12} \left| 1 - e^{-sT_{REF}} \right|^{2 \cdot (SD\text{ord}-1)}$$

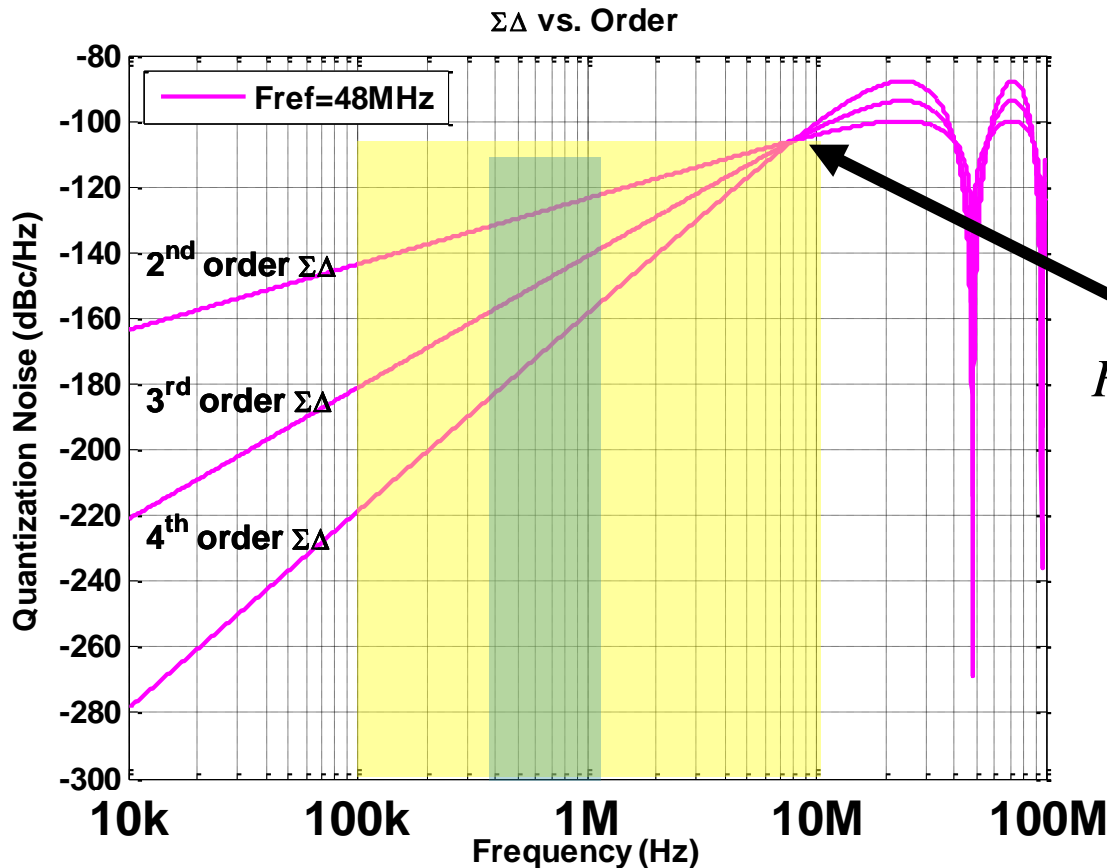


$$F_{cross} = \frac{\cos^{-1}(0.5)}{2\pi \cdot T_{REF}} = \frac{F_{REF}}{6} = 8\text{MHz}$$

**Going to higher order
suppresses $\Sigma\Delta$ noise
below F_{cross}**

What about $\Sigma\Delta$ Noise?

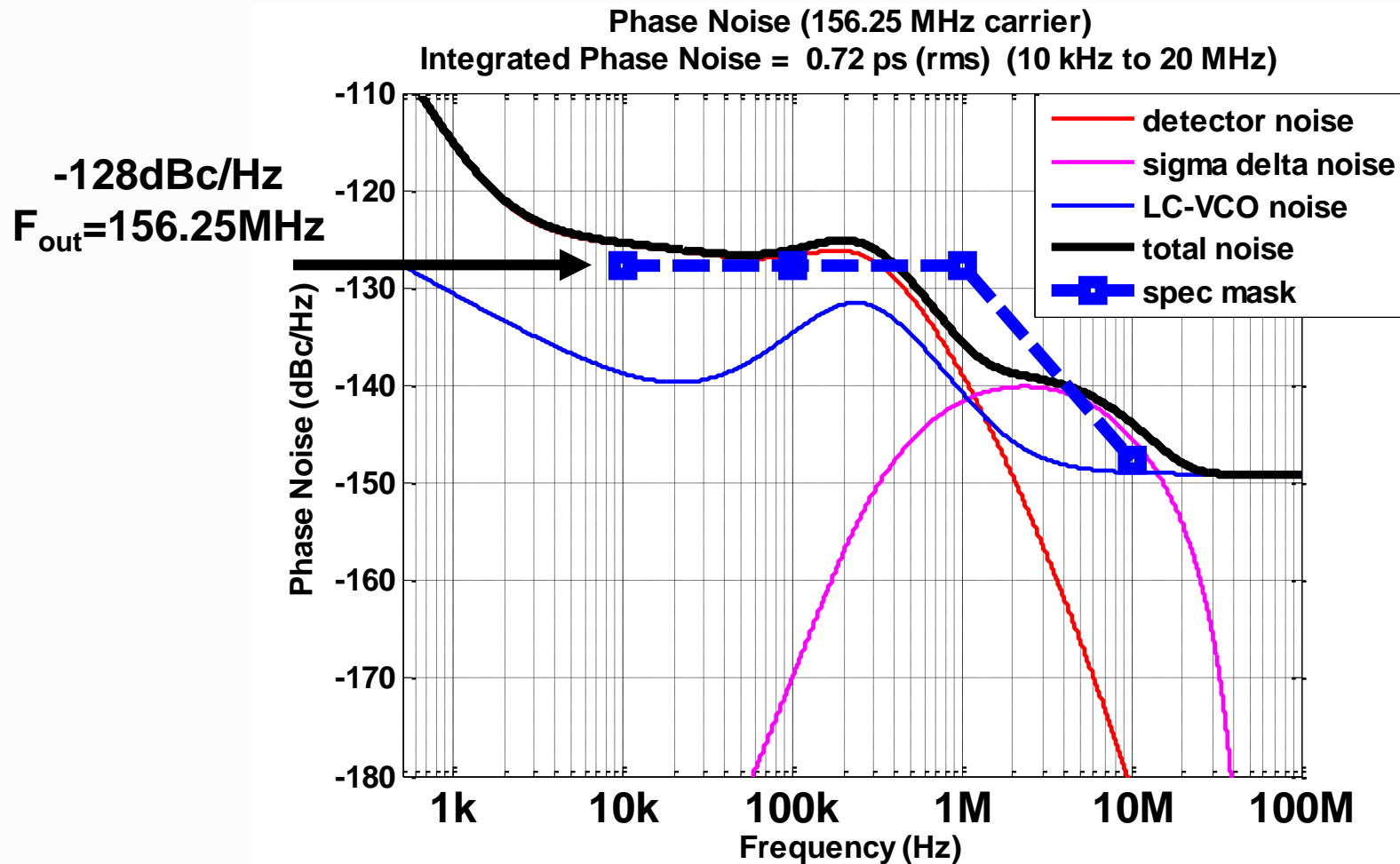
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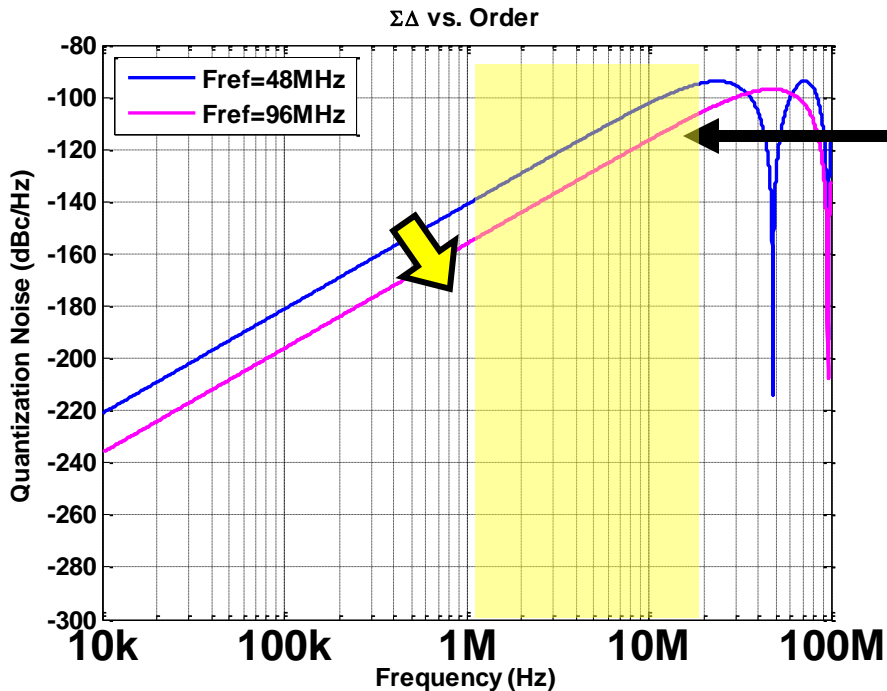
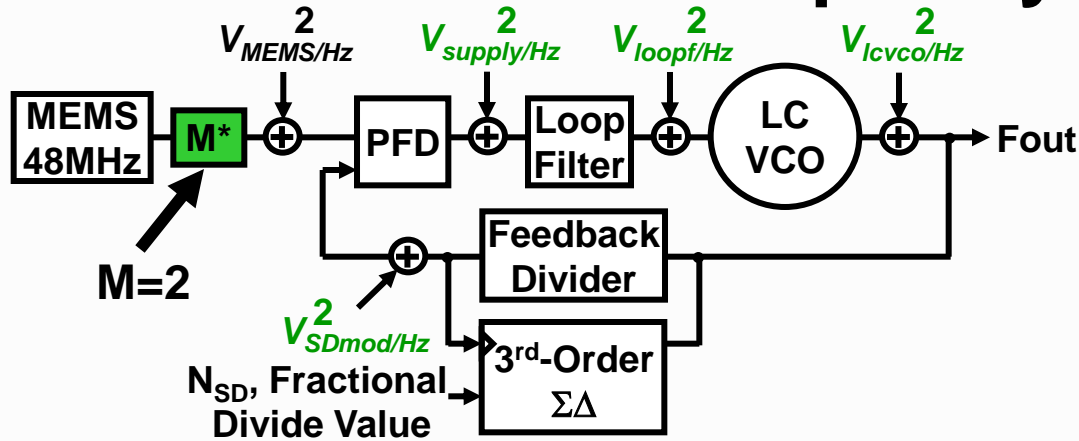
Going from 2nd to 3rd order $\Sigma\Delta$ will help in frequency of interest

FracN PLL with high (400kHz) PLL BW



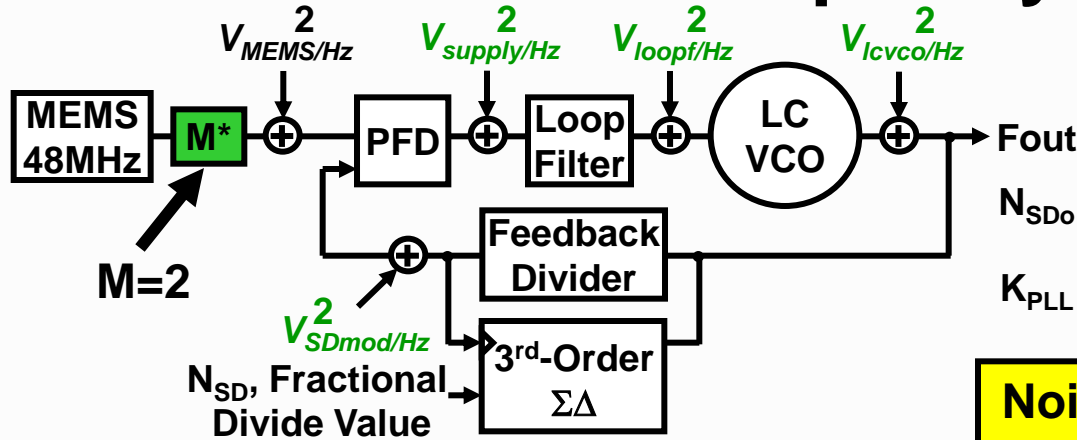
**Sub-ps jitter is met w/3rd order $\Sigma\Delta$
but phase noise mask is not... what else to do?**

Consider Frequency Doubler: M=2



$\Sigma\Delta$ now clocked at $2 \times 48\text{MHz} = 96\text{MHz}$

Consider Frequency Doubler: M=2



$$N_{SDo} = N_{SD} \text{ when } M=1$$

$$K_{PLL} = \frac{K_{PFD} * K_{vco} * LPF}{N_{SDo}}$$

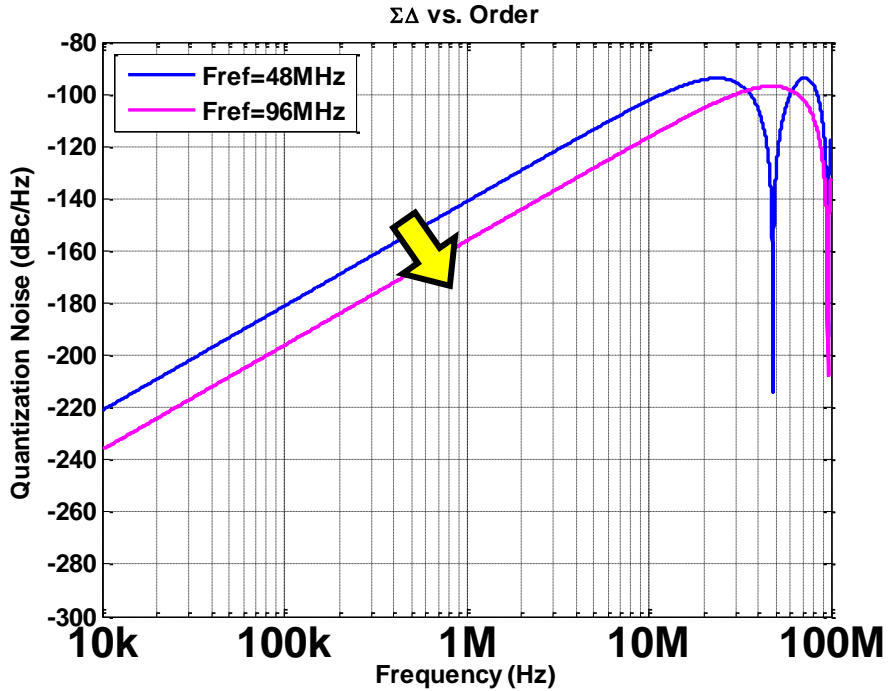
Noise Transfer Functions

$$\frac{V_{Fout/Hz}^2}{V_{supply/Hz}^2} = \frac{K_{PLL} * N_{SDo} / K_{PFD}}{S + K_{PLL} * M}$$

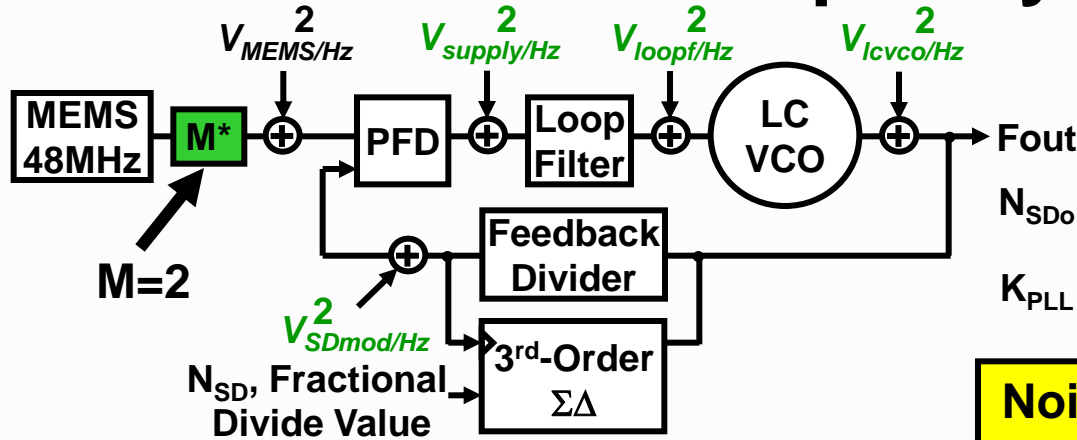
$$\frac{V_{Fout/Hz}^2}{V_{loopf/Hz}^2} = \frac{K_{PLL} * N_{SDo} / (K_{PFD} * LPF)}{S + K_{PLL} * M}$$

$$\frac{V_{Fout/Hz}^2}{V_{icvco/Hz}^2} = \frac{s}{S + K_{PLL} * M}$$

$$\frac{V_{Fout/Hz}^2}{V_{SDmod/Hz}^2} = \frac{K_{PLL} * N_{SDo}}{S + K_{PLL} * M}$$



Consider Frequency Doubler: M=2

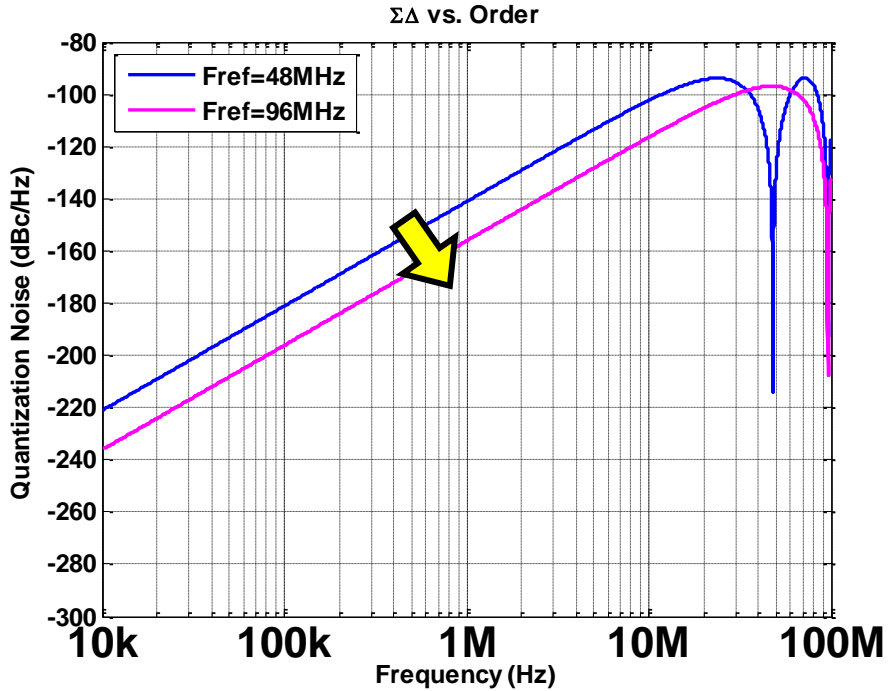


$$N_{SDo} = N_{SD} \text{ when } M=1$$

$$K_{PLL} = \frac{K_{PFD} * K_{VCO} * LPF}{N_{SDo}}$$

Noise Transfer Functions

In band gain: 6dB reduction when M=1 → 2



$$\frac{V_{Fout/Hz}^2}{V_{supply/Hz}^2} = \frac{K_{PLL} * N_{SDo} / K_{PFD}}{S + K_{PLL} * M}$$

$$\frac{N_{SDo}}{K_{PFD} * M}$$

$$\frac{V_{Fout/Hz}^2}{V_{loopf/Hz}^2} = \frac{K_{PLL} * N_{SDo} / (K_{PFD} * LPF)}{S + K_{PLL} * M}$$

$$\frac{N_{SDo}}{K_{PFD} * LPF * M}$$

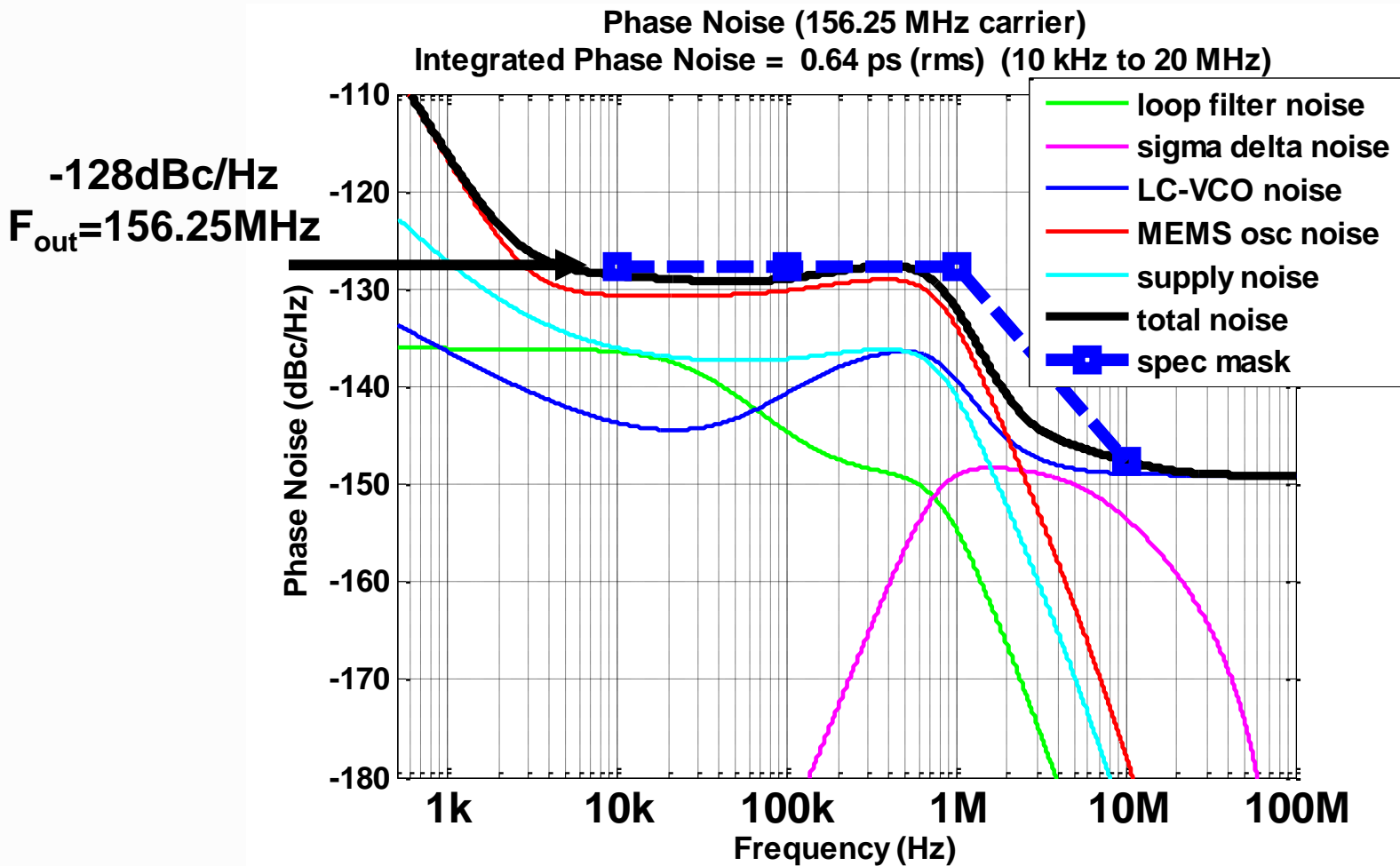
$$\frac{V_{Fout/Hz}^2}{V_{icvco/Hz}^2} = \frac{S}{S + K_{PLL} * M}$$

$$\frac{S}{K_{PLL} * M}$$

$$\frac{V_{Fout/Hz}^2}{V_{SDmod/Hz}^2} = \frac{K_{PLL} * N_{SDo}}{S + K_{PLL} * M}$$

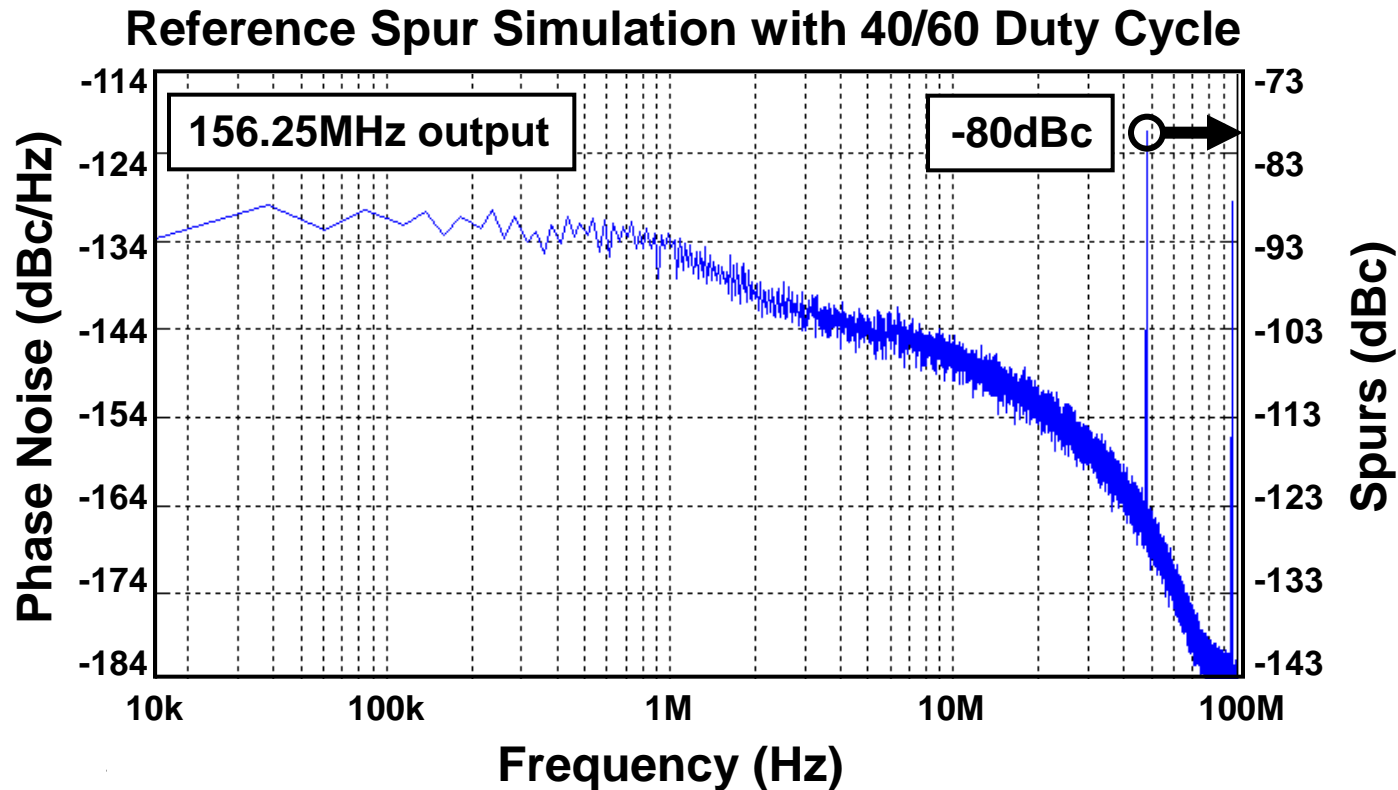
$$\frac{N_{SDo}}{M}$$

Phase Noise with Frequency Doubler



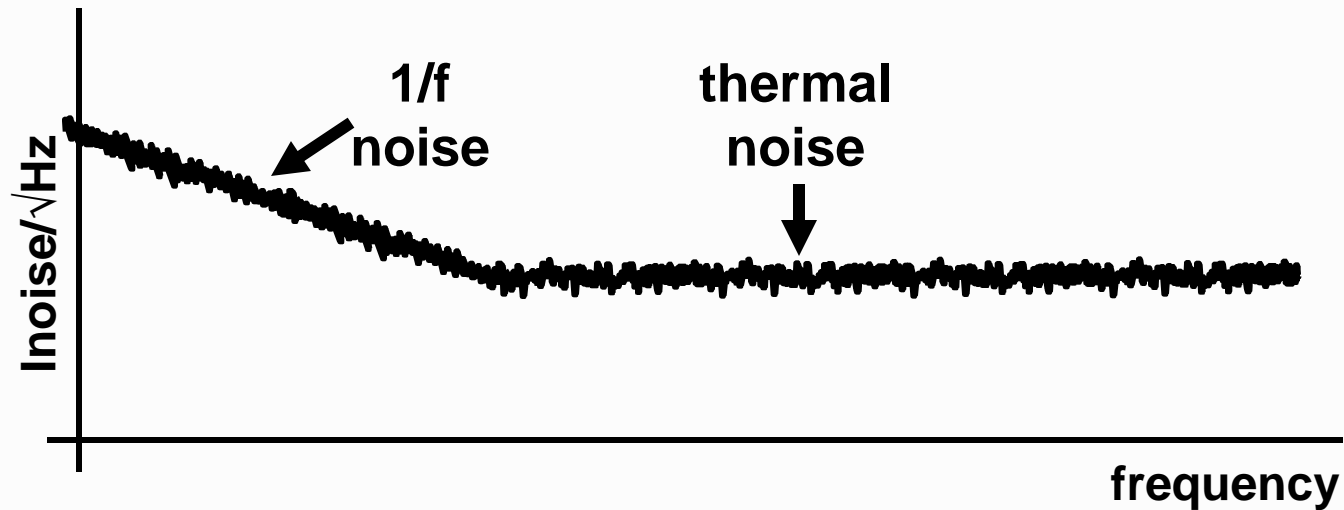
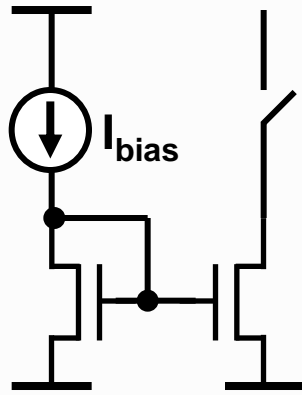
**Phase noise is under spectral mask
PLL bandwidth is also increased to ~1MHz**

Potential Risk of Doubler: Reference Spurs



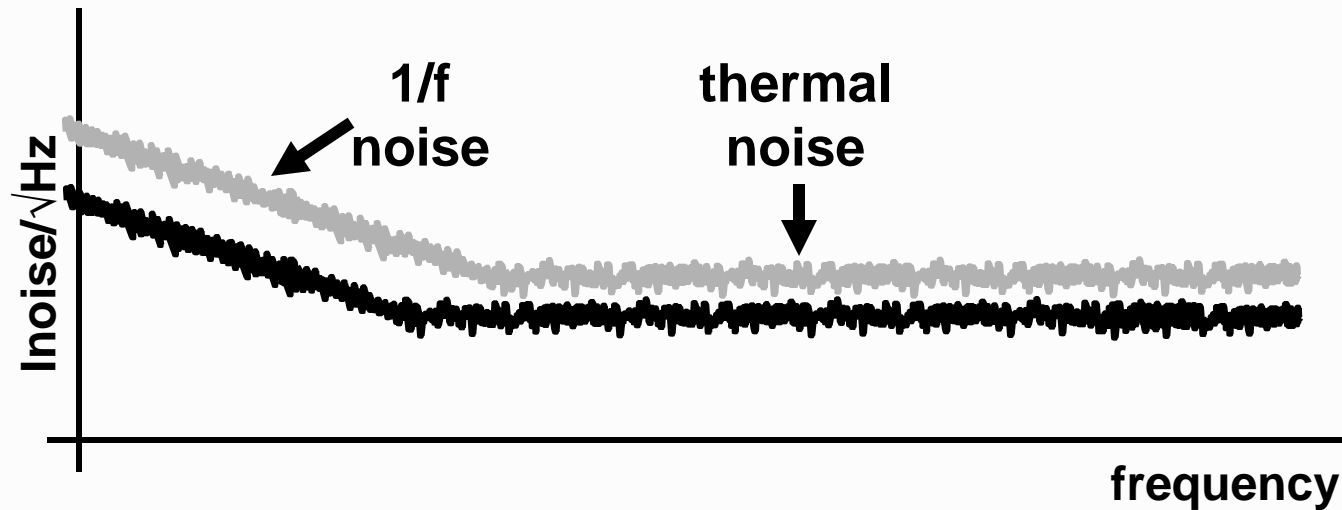
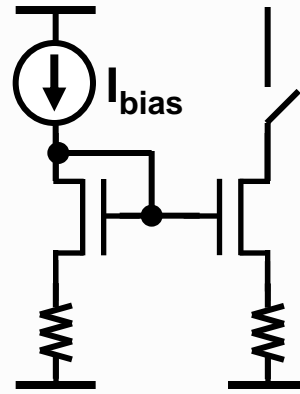
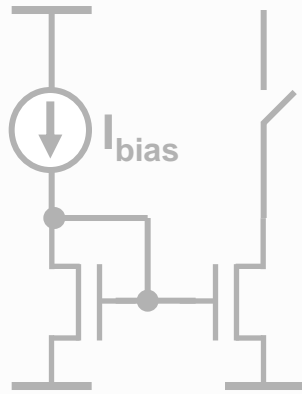
**Reference Spur @48MHz is <-80dBc @156.25MHz
Actual duty cycle much better than 40/60**

Evolution of a Charge Pump Current Source



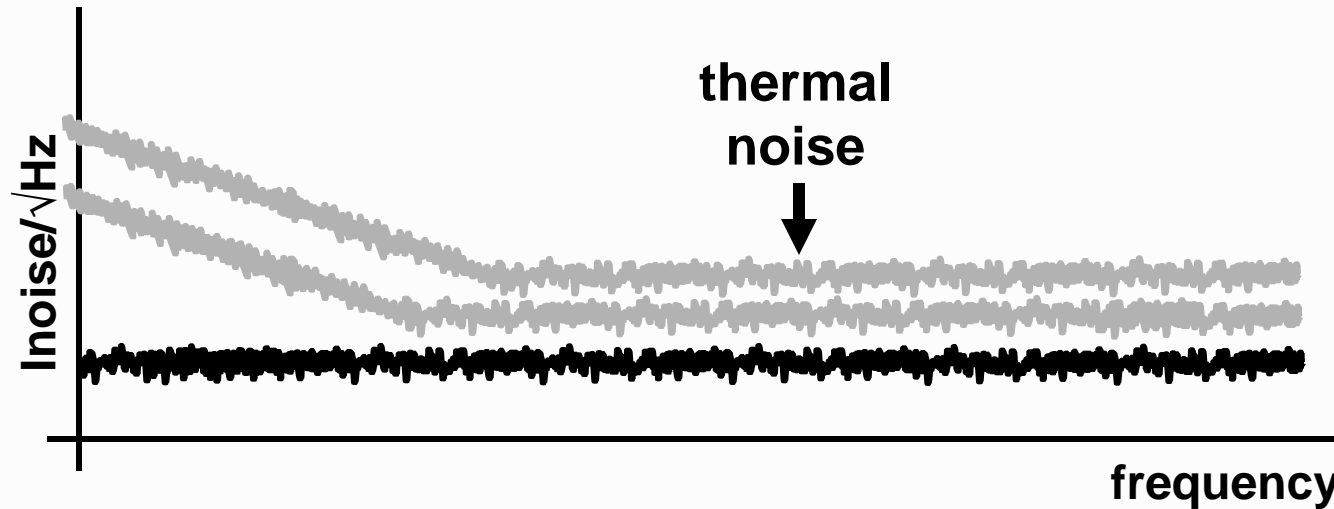
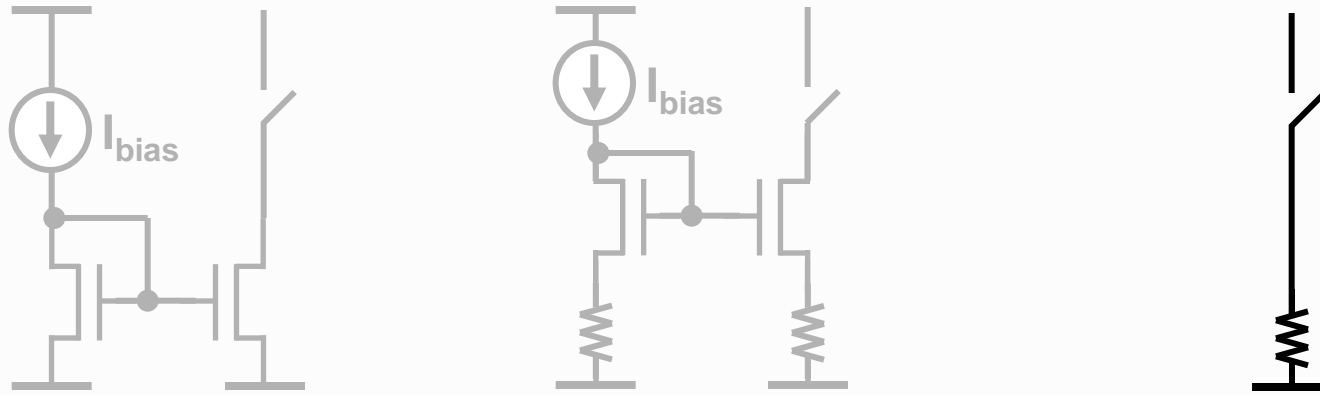
**Mostly transistor 1/f
and thermal noise**

Evolution of a Charge Pump: Degeneration



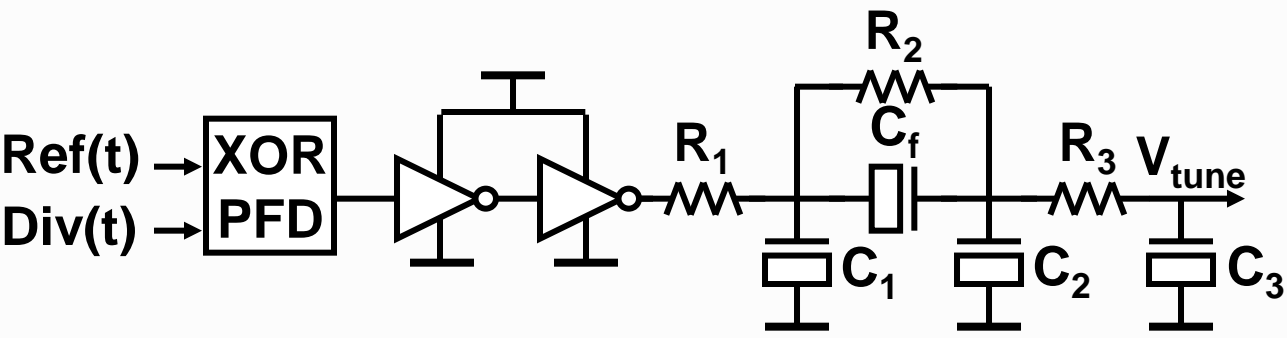
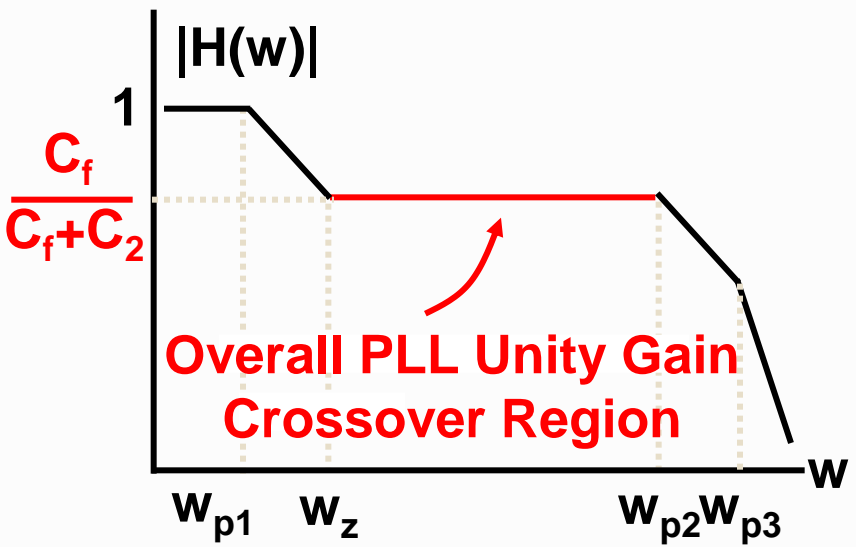
Degeneration reduces transistor noise and adds only thermal noise

Evolution of a Charge Pump: Switched Resistor



Switched resistor structure gives best noise performance at the cost of no charge pump gain

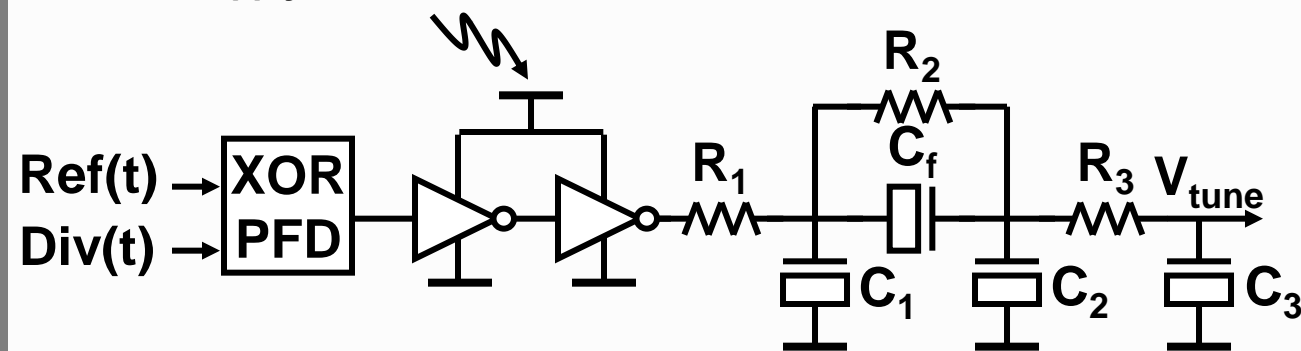
Switched-Resistor Loop Filter



Area saving accumulation NMOS varactors in passive loop filter

Switched-Resistor Loop Filter

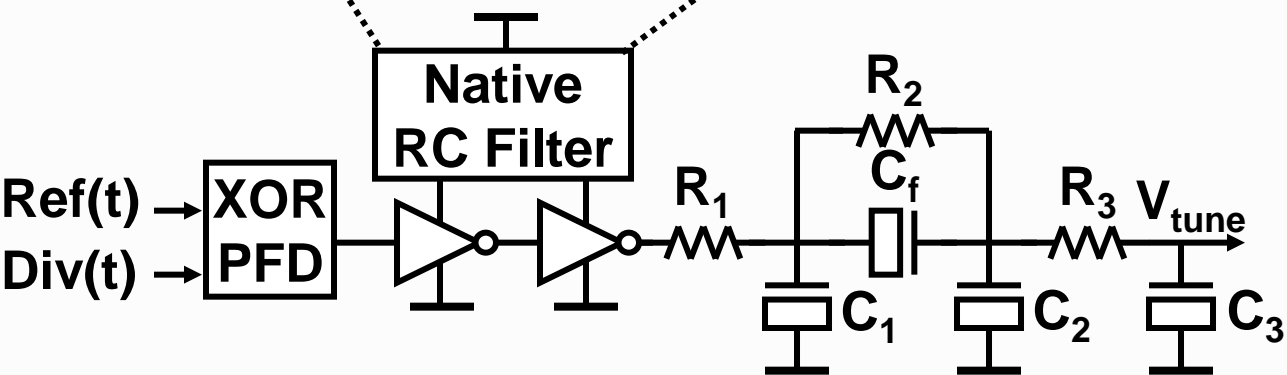
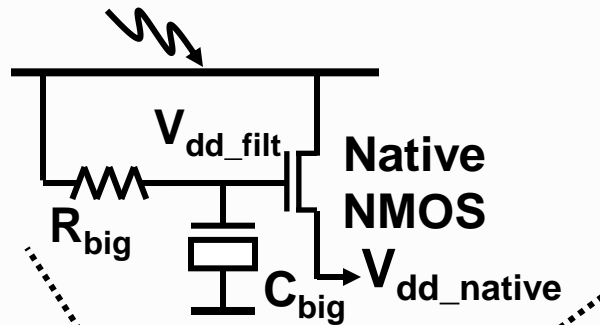
$$V_{\text{supply}/\sqrt{\text{Hz}}} = 60\text{nV}/\sqrt{\text{Hz}}$$



Supply Noise?

Native RC Filter

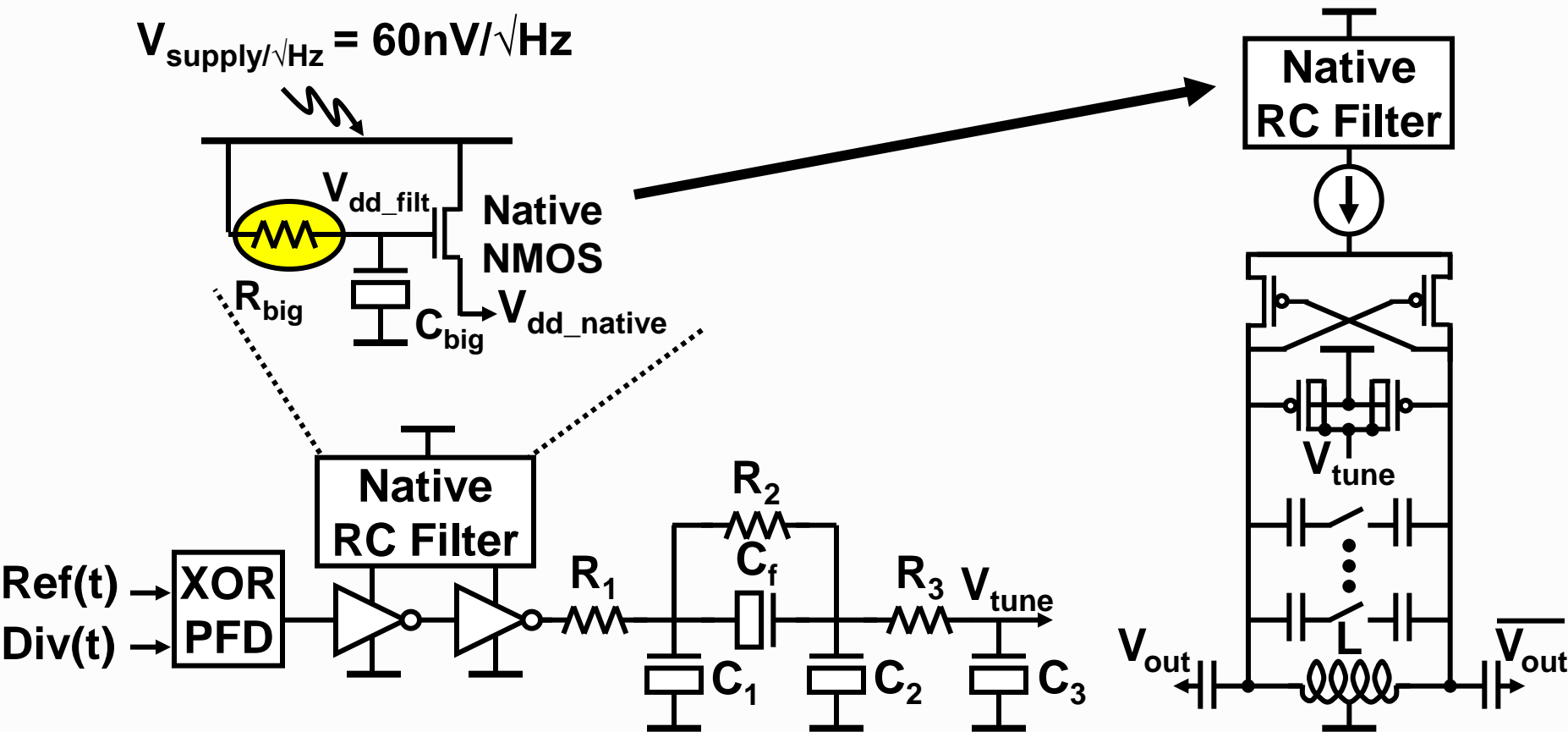
$$V_{\text{supply}/\sqrt{\text{Hz}}} = 60\text{nV}/\sqrt{\text{Hz}}$$



Native RC filter reduces supply noise

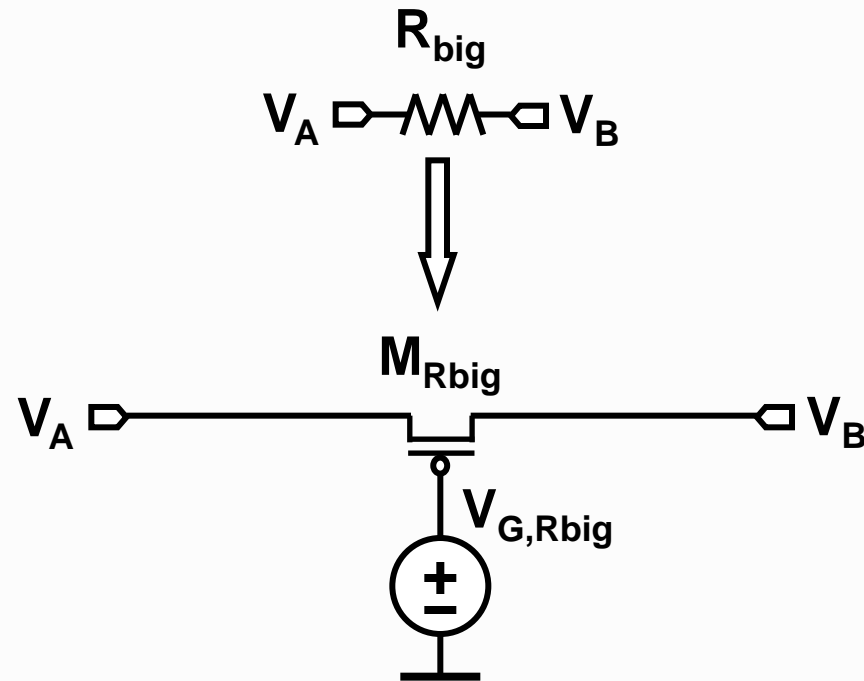
Loop Filter and LC-VCO

$$V_{\text{supply}/\sqrt{\text{Hz}}} = 60\text{nV}/\sqrt{\text{Hz}}$$



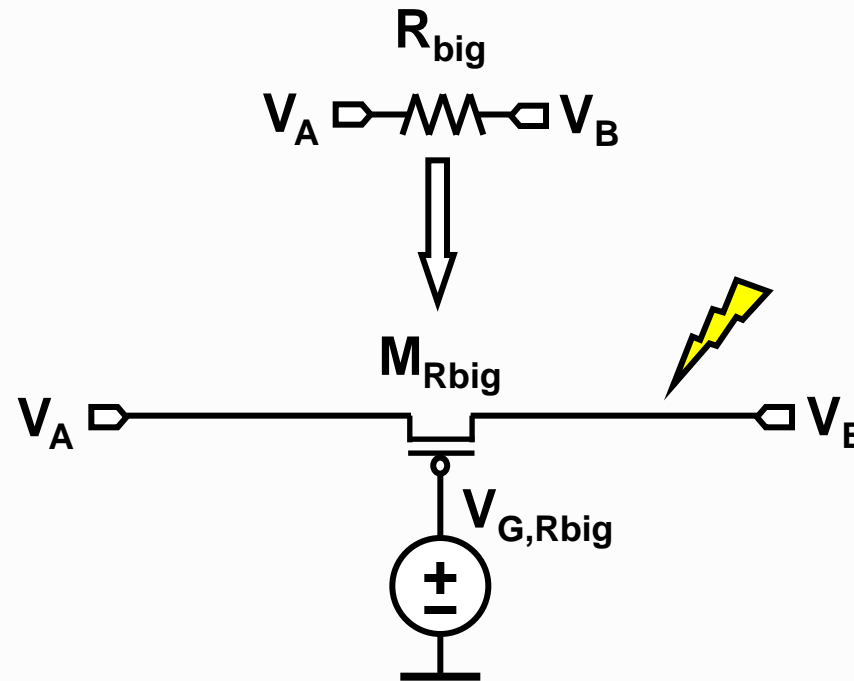
**Ground-based design reduces supply noise
All-PMOS VCO provides low 1/f noise**

Low Area R_{big} Active Resistor



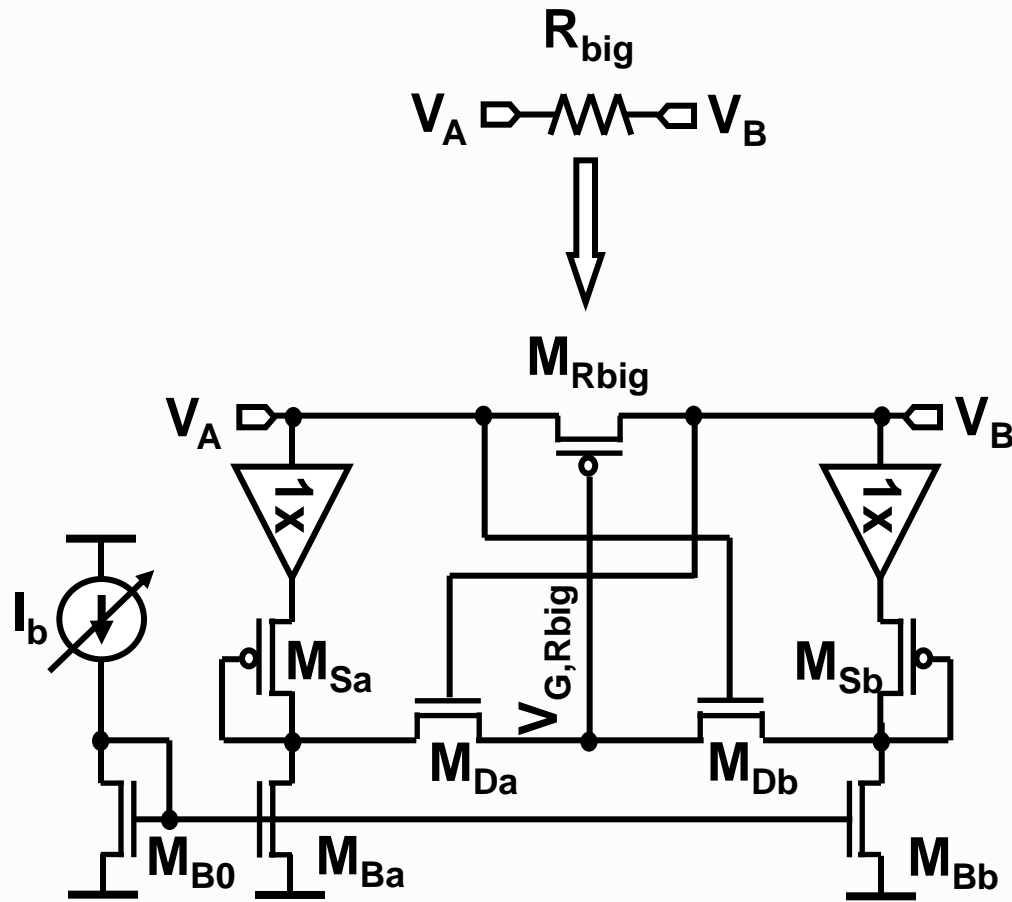
Active resistor reduces area requirement for $50\text{M}\Omega$ by 40x

Low Area R_{big} Active Resistor



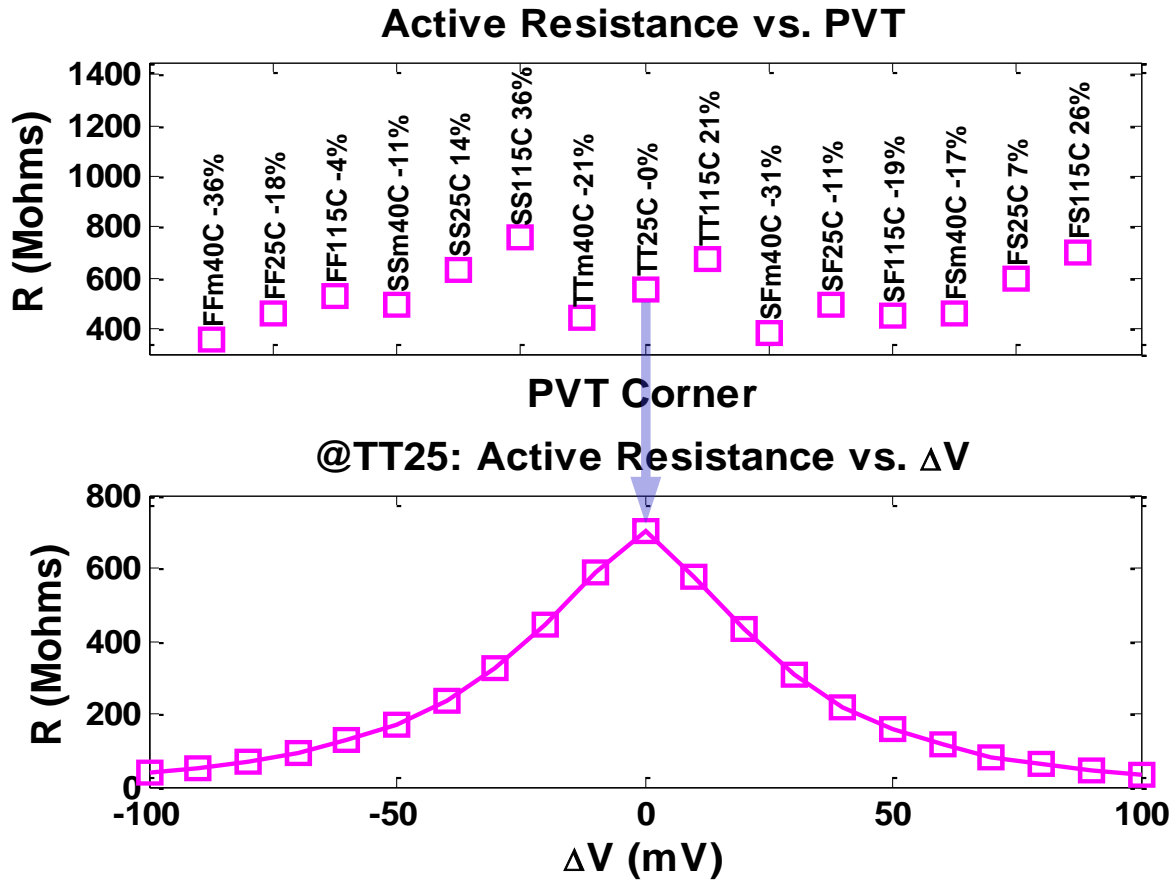
What happens if external electromagnetic (EM) coupling disturbs V_A or V_B ? Startup settling?

R_{big} EM coupling robustness and startup



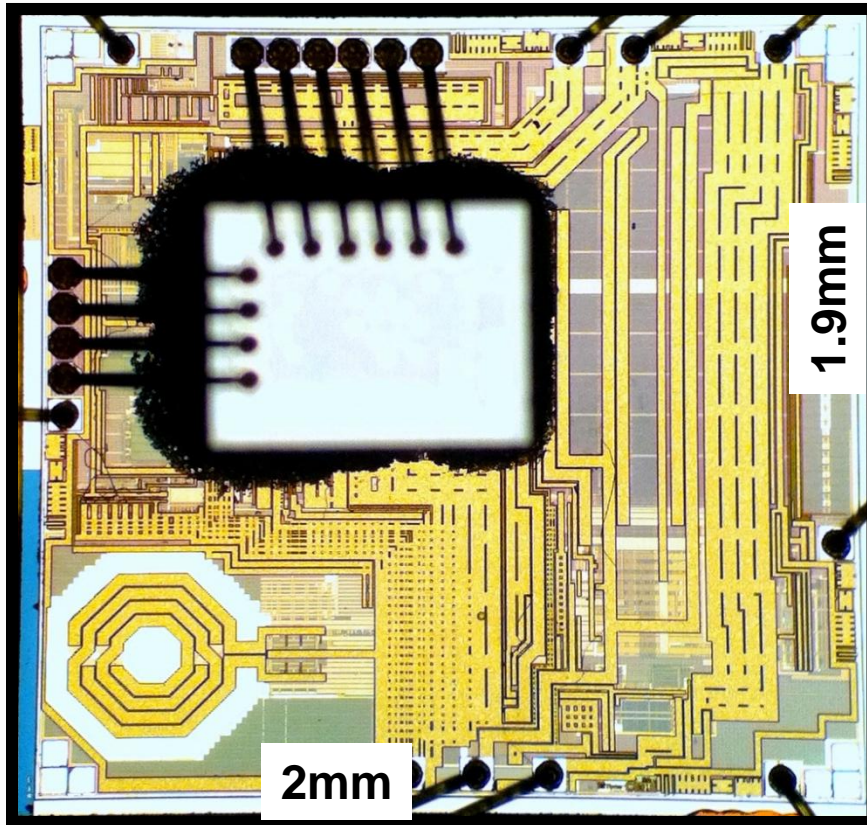
R_{big} gets smaller as $|V_A - V_B|$ gets bigger

R_{big} EM robustness and startup



**Only +/-36% variation over PVT (+/-25% for high- ρ poly).
EMI robustness: R decreases as $|\Delta V|$ increases.**

Die Photo and Measurement Summary



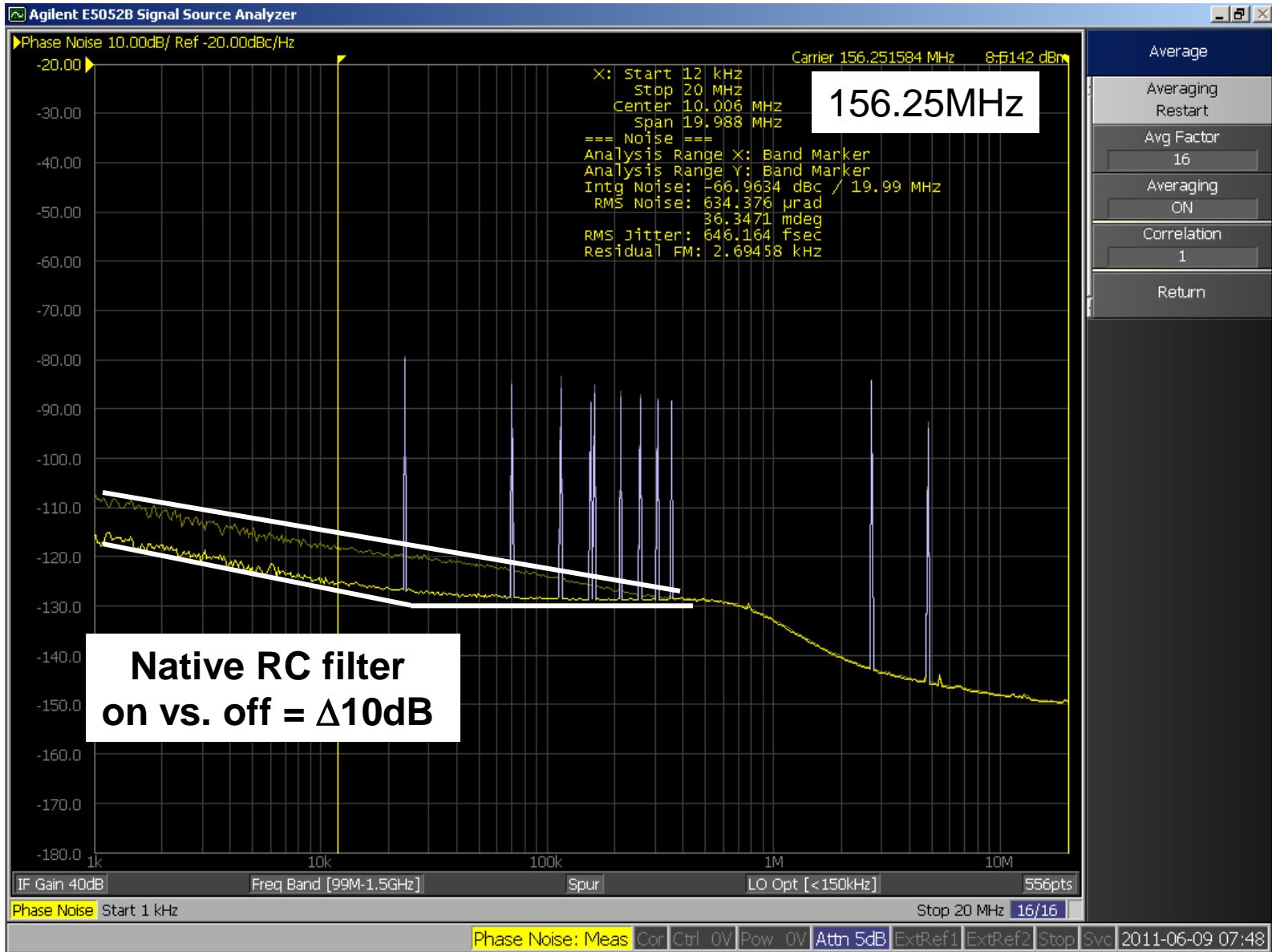
Vdd	1.71V-3.63V
Current	32mA
Temperature	-40C-90C
Area	2mm x 1.9mm
Fout	1MHz-260MHz
* FOM LC-VCO	180dBc/Hz/mW
Period Jitter	<4ps
** Integrated Jitter	600fs

* $FOM = 10 \cdot \log_{10}[(f_{vco}/f_o)^2/P(mW)] - PN(f_o)$

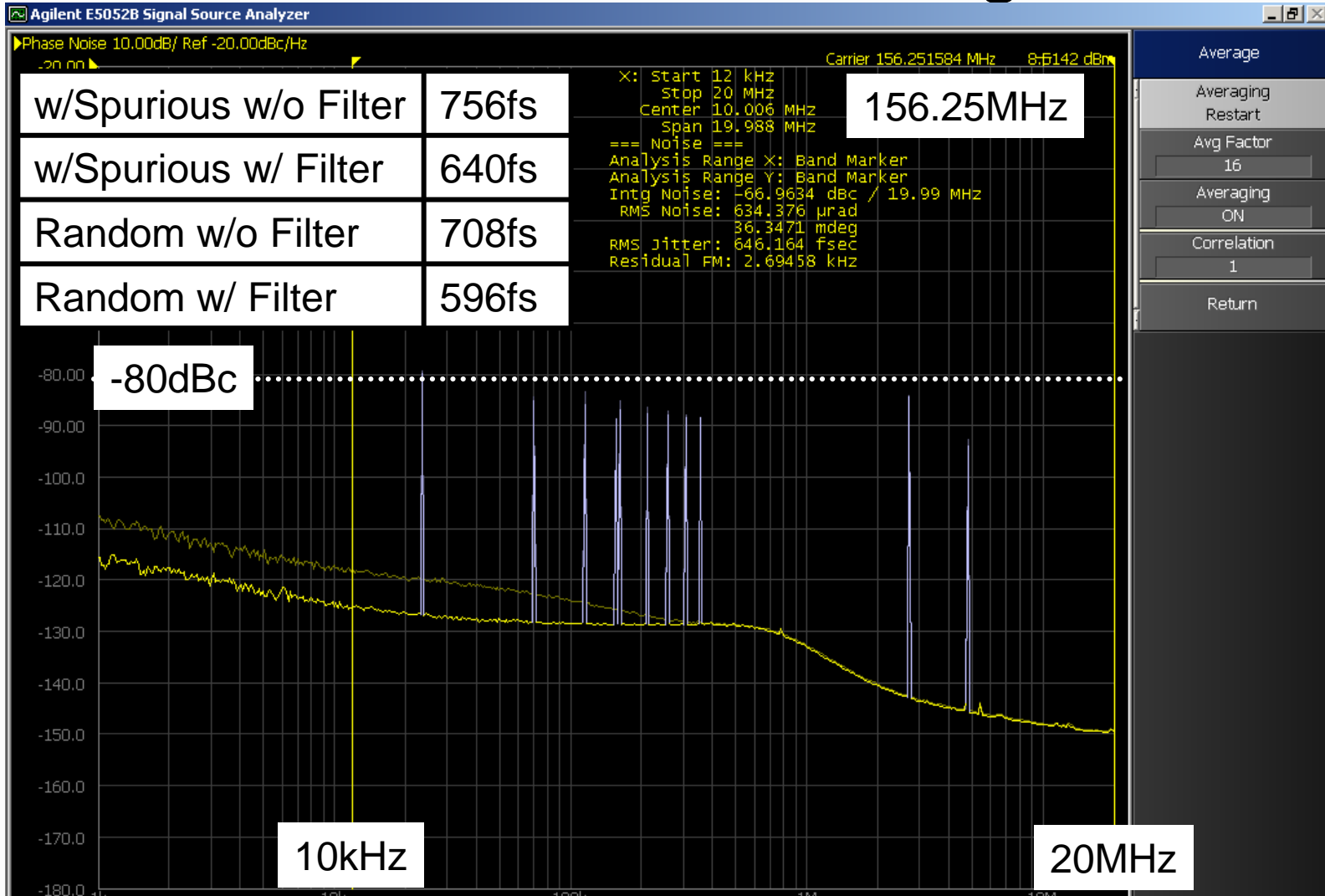
** From 10kHz to 20MHz

Achieved in a 4 pin 3225 QFN plastic package

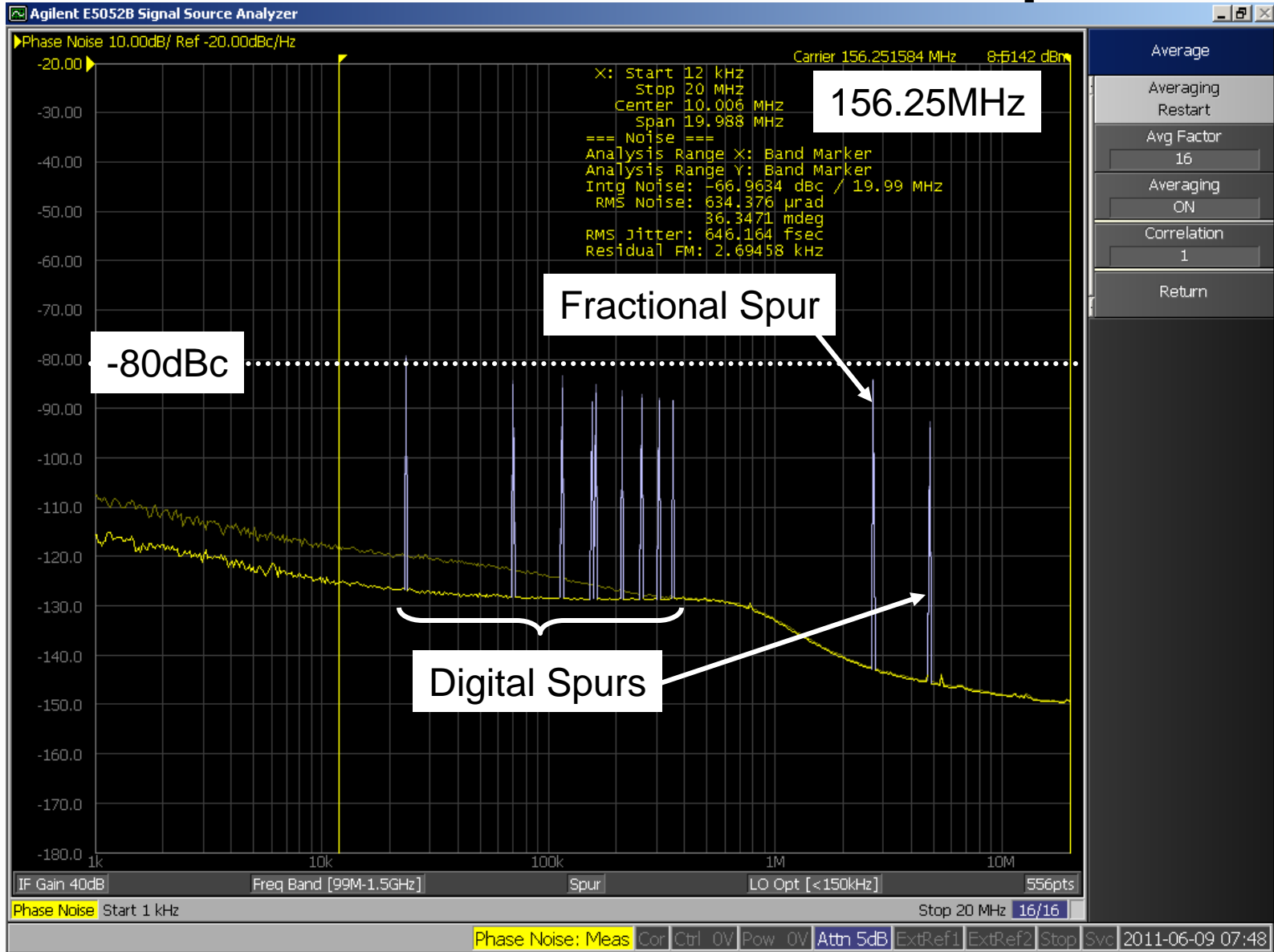
Phase Noise Measurement: Native RC Filter



Phase Noise Measurement: Integrated Jitter



Phase Noise Measurement: Spurs



Conclusions

MEMS-based timing references can achieve high-end quartz-like performance.

First MEMS-based clock generator to achieve an integrated phase jitter below 1ps (at 600fs), and a period jitter of <4ps.

The high bandwidth (1MHz) fractional-N PLL achieves this by leveraging:

- **Low noise 48MHz MEMS reference with doubler**
- **Low-noise PLL architecture and circuit techniques**

MEMS-based timing can now service high-speed digital communication standards such as SONET, 10Gb Ethernet, DSL, WiFi, and Femtocell applications.